Abstract of the Disclosure

There is provided a system and method for encoding and decoding of secured data. Decoding of secure data within a receive buffer is performed by a processor dedicated to that function. The processor accesses the data from a data port other than the bus used by a first processor. In this fashion, the data bus of the first processor is free for other operations while ciphering operations are underway. Also, the data is ciphered and hashed for data integrity in parallel to improve performance. Because the dedicated processor is not in direct communication with the data bus, it is clocked by a different clock and can therefore be designed economically to meet throughput requirements of a given system.